Claims 2, 10, 12 and 13 are rewritten to be in independent form and include all of the limitations of their base claims and any intervening claims. Claim 1 is amended.

The Office Action rejects claims 1 and 7-9 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,448,104 to Watanabe. If applicable to amended claims 1 and 7-9, this rejection is respectfully traversed.

Watanabe does not disclose, teach or suggest as sensor that includes "a photodiode region of a second conductivity type formed completely within the first well" as specified in claim 1, and therefore contained in claims 7-9 dependent on claim 1. This structure has advantages over Watanabe. For example, full containment of the photodiode region leads to full isolation of charge in the photodiode region from electrons outside of the photodiode region. Watanabe does not recognize this advantage, and absent recognition of this advantage, there is no motivation to modify the Watanabe structure to achieve the claim invention. Accordingly, withdrawal of the rejection of claims 1 and 7-9 is earnestly solicited.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Prompt reconsideration and allowance are earnestly solicited. Should the examiner believe that any further action is necessary to place the application in condition for allowance, the examiner is invited to contact the under signed at the telephone number listed below.

Respectfully submitted,

Date: **January 7, 2003**

Daniel E. Fisher

Daniel E. Fisher
Registration No. 34,162

DORSEY & WHITNEY LLP
Suite 400 South
1001 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Telephone: 202-442-3000
Facsimile: 202-442-3199

APPENDIX A

In this appendix, as required under 37 C.F.R. 1.121(c)(1)(i), is a clean version of the claims as amended without markings to indicate the changes that have been made, and with parenthetical expressions to indicate the status of the claim as amended or newly added.

1. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed completely within the first well.

2. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration;

a photodiode region of a second conductivity type formed in the first well; and

a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate.

10. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

A2 B1 Cont

a photodiode region of a second conductivity type formed in the first well,

wherein the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type in the second concentration.

12. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

B1

a photodiode region of a second conductivity type formed in the first well,

wherein the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type, and

A3

wherein the CMOS process type well is formed to a greater depth than a depth of the first well.

13. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed in the first well,

wherein the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type, and

wherein the CMOS process type well is formed to a greater concentration than the second concentration.

APPENDIX B

In this appendix, as required under 37 C.F.R. 1.121(c)(1)(ii), are the claims of the original specification which are marked up to show all the changes relative to the previous version of the claims. The changes are shown by brackets for deleted matter and underlining for added matter.

1. (Amended) A sensor formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed [in] completely within the first well.

2. (Amended) [The] A sensor [of claim 1, further comprising] formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration;

a photodiode region of a second conductivity type formed in the first well; and

a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate.

10. (Amended) [The] A sensor [of claim 1] formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed in the first well,

wherein the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type in the second concentration.

12. (Amended) [The] A sensor [of claim 1] formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed in the first well,

wherein[:] the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type[;], and

wherein the CMOS process type well is formed to a greater depth than a depth of the first well.

13. (Amended) [The] A sensor [of claim 1] formed in a substrate of a first conductivity type in a first concentration comprising:

CMOS circuitry to control the sensor;

a first well of the first conductivity type in a second concentration formed in the substrate, the second concentration being greater than the first concentration; and

a photodiode region of a second conductivity type formed in the first well,

wherein[:] the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type[;], and

wherein the CMOS process type well is formed to a greater concentration than the second concentration.